ABSTRACT

The present invention relates to a semicustom ASIC, in which a plurality of standard cell rows are arranged. The standard cell and basic cells used in a gate array are mixedly mounted on the same chip. Respective cell rows are composed of a plurality of standard cells with an empty space. The basic cells used in the gate array are arranged as dummy cells. They are disposed in wiring channel regions between the plurality of standard cells or empty spaces between the standard cells in a same standard cell row. Only the latter may be used if the channelless type standard cells are employed. A changing request can be satisfied by forming metal wiring layers on the gate array basic cells when there is a necessity of changing circuit design or pattern. Since the circuit can be modified without change of gate polysilicon regions and source/drain regions underlying the metal wiring layers, design and manufacture can be effected in a short period of time.